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HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
P.O. Box 272400  
Fort Collins, CO 80527-2400

EXAMINER

QUILLEN, ALLEN E

ART UNIT

PAPER NUMBER

2676

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7

Please find below and/or attached an Office communication concerning this application or proceeding.

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## Office Action Summary

Application No.

09/715,746

Applicant(s)

LEFEBVRE ET AL.

Examiner

Allen E. Quillen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 14 May 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☒ Claim(s) 12 and 17 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Response to Amendment*

1. Claims 1, 7-14 are amended, 15-25 added. All claims pending. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

### *Double Patenting*

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 2, 6-8, 11-12 are provisionally rejected under the judicially created doctrine of provisional obviousness-type double patenting as being unpatentable over claims 1, 7, 11 and 12 of copending Application No. 09/715253. Claims 3-5, 9-10, 13-14 are provisionally rejected under the judicially created doctrine of provisional obviousness-type double patenting as being unpatentable over claims 4, 7 and 9 of copending Application No. 09/715335. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented. The conflicting claims are not identical; they are patentably distinct from each other because

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current application 09/715,746 additionally recites "plurality of display devices". Applications No. 09/715253 and Application No. 09/715335 do not recite "plurality of display devices". At the time of the invention, it would have been obvious to one skilled in the art of computer graphics processing to use a plurality of displays to achieve a larger-sized display.

### *Claim Objections*

4. In the Amendment, page 17 and 20, Claims 12 and 17 are objected to because of the following informalities. Examiner objects: (1) page 20, claim numbered "12" (should be "7" according to a telephone conversation with the Applicant's Attorney, Mr. Jon Holland, July 29, 2003, 1:25pm EDT); and page 6, amended claim 17, line 4, an extra preposition, "in" in the claim language (...with respect to an in image defined by...). Therefore, on the above basis, Examiner proceeds with the examination; and, on page 20 of the Response, Claim 12 is re-numbered to 7. Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis, et al, U.S. Patent 6,573,905 in view of Computer Wall II, RGB Spectrum, Inc., Specifications, 950 Marina Village Parkway, Alameda, CA 94501, 9/2000, available on the world wide web at: <http://www.rgb.com/Webpages/prodpgs/cwall.html>,

7. Regarding claim 1, MacInnis discloses a single graphical display system ( Figures 1-7, 48, 60-64, 69-70, 73-74; Column 6, lines 21, 29-33), comprising: an interface configured to receive graphical data defining an image (Column 5, lines 7-20, 34-37, 45-49); and a plurality of

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graphical acceleration units (Figure 2, element 64; Figure 37, element 64; *completely contained in an integrated chip*, Column 59, lines 10-12; *..the system may be implemented using two or more separate integrated circuit chips*, Column 61, lines 29-56; *four independent graphics conversion pipelines*, Figure 69, Column 112, lines 24-33), each of said plurality of graphical acceleration units respectively interfaced with one of said plurality of displays and configured to render a portion of said graphical data to said one display device such that said display displays said image as a single screen (*window descriptors, list*, Column 13, lines 1-33), wherein at least one of said graphical acceleration units comprises: a first graphical pipeline configured to render graphical data (Figure 69, Column 112, lines 24-33); a second graphical pipeline configured to render graphical data (see above, Figure 69, Column 112, lines 24-33); second display means for displaying a second image based on said composited portion (*video pipeline*, Figure 4, Column 6, lines 53-60; Column 7, lines 4-10, 16-20); and a compositor configured to interface with said one display said graphical data rendered by said first and second graphical pipelines (see above; Figure 62, 69; Column 52, lines 18-19; Column 52, lines 19-23; Column 46, lines 1-7; ).

MacInnis does not disclose a single logical screen (SLS) graphical display system comprising a plurality of display devices. RGB Spectrum Specification teaches the single logical screen (SLS) graphical display system comprising a plurality of display devices (*video wall*, page 1, lines 4-9). The motivation for combining graphics pipeline processing and video compositing with a video wall is for high resolution imagery for large display walls used in data assessment and decision making for real-time command, control and communications and control rooms (RGB Spectrum, page 1). RGB Spectrum Specification is evidence that, at the time of the invention, it would have been obvious for someone skilled in the art of graphical and

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video data digital display processing to combine the benefits of interfacing, pipeline processing using multiple pipelines and video compositing, as MacInnis discloses, with multiple displays, as the RGB Spectrum Specification teaches, to provide for large video walls for data assessment and decision making.

8. Regarding claim 2, MacInnis discloses the system of claim 1, wherein: said first graphical pipeline is configured to mathematically combine a first offset (*upper and lower layers*, Column 48, line 35 through Column 49, line 10) with coordinate values included in said graphical data rendered by said first graphical pipeline; said second graphical pipeline is configured to mathematically combine a second offset with coordinate values included in said graphical data rendered by said second graphical pipeline; and said compositor is configured to blend color values associated with corresponding coordinate values within said graphical data rendered by said first and second graphical pipelines (see above, Column 49, lines 1-17; *vector processor, mathematically, arithmetic*, Column 59, lines 20-28; Column 66, lines 37-45; Column 109, lines 21; Column 48, line 4; Column 16, line 60 through Column 17, line 6).

9. Regarding claim 3, representative of claims 4, MacInnis discloses the system of claim 1, wherein said first graphical pipeline is configured to discard said graphical data rendered by said second graphical pipeline, and wherein said second graphical pipeline is configured to discard said graphical data rendered by said first graphical pipeline (see above, Figure 69, Column 112, lines 24-33; Column 8, lines 7-9; Column 16, lines 47-50).

***Claim Rejections - 35 USC § 103***

10. Claims 5-16, 18-19, 21, 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis, et al, U.S. Patent 6,573,905 in view of Computer Wall II, RGB Spectrum, Inc., Specifications, 950 Marina Village Parkway, Alameda, CA 94501, 9/2000, available on the world wide web at: <http://www.rgb.com/Webpages/prodpgs/cwall.html>, and, in further view of Jenkins, U.S. Patent 6,111,582.

11. Regarding claim 5, MacInnis discloses the system of claim 3, wherein said first graphical pipeline is further configured to super sample said graphical data rendered by said first graphical pipeline, and wherein said second graphical pipeline is further configured to super sample said graphical data rendered by said second graphical pipeline (see above, *post filtering, digitized analog video capture*, Column 5, lines 56-61; Column 9, lines 46-55).

MacInnis does not disclose multiple rendering means nor a second image or portion of the image. Jenkins teaches multiple pipelines (Column 60, lines 29-63); wherein said first and second images define at least a portion of a image; second rendering means for rendering a respective second portion of said graphical data, said second rendering means including a plurality of pipeline means for rendering said second graphical data portion in parallel and a compositing means for compositing said second rendered portion (Figures 1-4, Figure 13A, *sub-images, being handled by one of the sub-image processors*, Column 17, lines 52-55). The motivation for combining multiple pipeline processing with multiple sub-images with respective rendering means is for efficient use of available connection bandwidth and allow rapid



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synchronization with broadcast event stream, load balancing, computational efficiency, level of detail and resolution suited to human needs (Column 114, lines 51-54, 63-63; Column 117, lines 1-6, 24, 38-40, 48-50, 63-67, Column 118, lines 1-9, 17-28, 36-38, 55-65). Jenkins is evidence that at the time of the invention it would have been obvious to one skilled in the art of computer graphics processing to combine the benefits of parallel pipeline processing, as MacInnis discloses, with multiple sub-images rendering, as Jenkins teaches, for performance and display efficiencies.

12. Regarding claim 6, MacInnis discloses the system of claim 5, wherein said compositor is configured to blend color values included in said graphical data rendered by said first and second graphical pipelines (see above, Column 16, lines 14-25; Figures 28-30, Column 10, line 41 through Column 11, line 39).

13. Regarding Claim 7, representative of claims 11, 18, 21, 23-25, MacInnis discloses a graphical display system, comprising: means for receiving a graphical command (*LOAD*, Column 59, lines 21-34); first rendering means for rendering a first portion of graphical data included within said graphical command, said first rendering means including a plurality of pipeline means for rendering said first graphical data portion in parallel and a compositing means for compositing said first rendered portion (see above, Figure 69, Column 112, lines 24-33); first display means for displaying a first image based on said composited portion(see above, Column 52, lines 18-19); [Claim 11, wherein a plurality of graphical acceleration units (see above),

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compositing the graphical data rendered by said at least one graphical acceleration unit (see above).

MacInnis does not disclose single logical screen (SLS) graphical display system. RGB Spectrum Specification teaches the single logical screen (SLS) graphical display system comprising a plurality of display devices (video wall, page 1, lines 4-9). The motivation for combining graphics pipeline processing and video compositing with a video wall is for high resolution imagery for large display walls used in data assessment and decision making for real-time command, control and communications and control rooms (RGB Spectrum, page 1). RGB Spectrum Specification is evidence that, at the time of the invention, it would have been obvious for someone skilled in the art of graphical and video data digital display processing to combine the benefits of interfacing, pipeline processing using multiple pipelines and video compositing, as MacInnis discloses, with multiple displays, as the RGB Spectrum Specification teaches, to provide for large video walls for data assessment and decision making.

MacInnis discloses multiple pipelines (Column 112, lines 24-33) but does not disclose multiple rendering means nor a second image or portion of the image. Jenkins teaches multiple pipelines (Column 60, lines 29-63); wherein said first and second images define at least a portion of a image; second rendering means for rendering a respective second portion of said graphical data, said second rendering means including a plurality of pipeline means for rendering said second graphical data portion in parallel and a compositing means for compositing said second rendered portion (Figures 1-4, Figure 13A, *sub-images, being handled by one of the sub-image processors*, Column 17, lines 52-55). The motivation for combining multiple pipeline processing with multiple sub-images with respective rendering means is for efficient use of

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available connection bandwidth and allow rapid synchronization with broadcast event stream, load balancing, computational efficiency, level of detail and resolution suited to human needs (Column 114, lines 51-54, 63-63; Column 117, lines 1-6, 24, 38-40, 48-50, 63-67, Column 118, lines 1-9, 17-28, 36-38, 55-65). Jenkins is evidence that at the time of the invention it would have been obvious to one skilled in the art of computer graphics processing to combine the benefits of parallel pipeline processing, as MacInnis discloses, with multiple sub-images rendering, as Jenkins teaches, for performance and display efficiencies.

14. Regarding claim 8, representative of claims 9, 10, 13, 14, MacInnis discloses the system of claim 7, wherein each of said plurality of pipeline means of said first rendering means includes a means for mathematically combining a different offset to coordinate values included in said first graphical data portion, and wherein said compositing means of said first rendering means includes a means for blending color values associated with corresponding coordinate values within said first graphical data portion; [Claim 9] wherein said first rendering means includes a means for receiving an input identifying a coordinate range, and wherein one of said plurality of pipeline means of said first rendering means includes a means for discarding graphical data from said first graphical data portion based on said coordinate range (see above; Figure 15, Column 31, lines 34-64; *vector processor, mathematically, arithmetic*, Column 59, lines 20-28; Column 66, lines 37-45; Column 109, lines 21; Column 48, line 4; Column 16, line 60 through Column 17, line 6).

MacInnis discloses multiple pipelines (Column 112, lines 24-33) but does not disclose multiple rendering means nor a second image or portion of the image. Jenkins teaches multiple

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pipelines (Column 60, lines 29-63); wherein said first and second images define at least a portion of a image; second rendering means for rendering a respective second portion of said graphical data, said second rendering means including a plurality of pipeline means for rendering said second graphical data portion in parallel and a compositing means for compositing said second rendered portion (Figures 1-4, Figure 13A, *sub-images, being handled by one of the sub-image processors*, Column 17, lines 52-55). The motivation for combining multiple pipeline processing with multiple sub-images with respective rendering means is for efficient use of available connection bandwidth and allow rapid synchronization with broadcast event stream, load balancing, computational efficiency, level of detail and resolution suited to human needs (Column 114, lines 51-54, 63-63; Column 117, lines 1-6, 24, 38-40, 48-50, 63-67, Column 118, lines 1-9, 17-28, 36-38, 55-65). Jenkins is evidence that at the time of the invention it would have been obvious to one skilled in the art of computer graphics processing to combine the benefits of parallel pipeline processing, as MacInnis discloses, with multiple sub-images rendering, as Jenkins teaches, for performance and display efficiencies.

15. Regarding claim 12, MacInnis discloses the method of claim 11, wherein said rendering further comprises mathematically combining different offsets with coordinate values included in one of said graphical data portions, and wherein said compositing comprises blending color values associated with said coordinate values (see above, Column 49, lines 1-17; *vector processor, mathematically, arithmetic*, Column 59, lines 20-28; Column 66, lines 37-45; Column 109, lines 21; Column 48, line 4; Column 16, line 60 through Column 17, line 6).

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16. Regarding claim 15, MacInnis discloses the system of claim 1, wherein each of the portions of said graphical data rendered by said plurality of graphical acceleration units is included in a single graphical command ((*LOAD*, Column 59, lines 21-34).

17. Regarding claim 16, representative of claim 19, MacInnis discloses the system of claim 1, further comprising a graphics application (*Direct Draw*, Column 62, lines 33-35), wherein each of the portions of said graphical data rendered by said plurality of graphical acceleration units is transmitted from said graphics application (Column 112, lines 24-33).

***Claim Rejections - 35 USC § 103***

18. Claims 17, 20, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis, et al, U.S. Patent 6,573,905 in view of Computer Wall II, RGB Spectrum, Inc., Specifications, 950 Marina Village Parkway, Alameda, CA 94501, 9/2000, available on the world wide web at: <http://www.rgb.com/Webpages/prodpgs/cwall.html>, in further view of Deering, U.S. Patent 6,496,186, and Dachille, et al, GI-Cube: An Architecture for Volumetric Global Illumination and Rendering, SIGGRAPH/EUROGRAPHICS Workshop on Graphics Hardware, August 2000, Interlaken Switzerland, ACM Press, NY, NY, pages 119-128

19. Regarding claim 17, representative of claims 20, 22, MacInnis discloses the system of claim 2, wherein said first and second graphical pipelines, by respectively combining said first and second offsets with coordinated values in said graphical data rendered by said first and

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second graphical pipelines, offsets an image defined by said graphical data rendered by said first graphical pipeline with respect to an image defined by said graphical data rendered by said second graphical pipeline such that said compositor defines a jitter enhanced image by blending said color values (*window descriptors, list*, Column 13, lines 1-33); [Claim 22, wherein one of said graphical acceleration units comprises a plurality of graphical pipelines, each of said graphical pipelines configured to mathematically combine a different offset to corresponding coordinate values of the graphical data portion rendered by said one graphical acceleration unit such that the compositor of said one graphical acceleration unit jitter enhances an image defined by said graphical data portion rendered by said one graphical acceleration unit (see above).

MacInnis does not disclose jitter enhanced. [ Examiner takes notice that the use of the term “jitter” can have multiple distinct meanings, for example, (1) frame to frame “jiggling”, an undesired effect, (see below, Deering, Column 15, lines 54-65), (2) creating special desired effects (see below, Deering, Column 2, lines 38-60), and (3) a graphics rendering image enhancement method as documented in the literature related to reducing aliasing, a stair-stepping effect along a smooth line or curve, caused by display method limitations (see Deering and Dachille below). ]

MacInnis does not explicitly disclose wherein said compositor defines a jitter enhanced image ([instant application: *...each pipeline 56-59 adds a small offset to the coordinates of each pixel rendered by the pipeline...offsets...can be randomly generated by each pipeline and/or can be pre-programmed into each pipeline 56-59..* Page 29, lines 14-18]. Deering teaches supersampling and filtering in the context of Applicant’s specification (Column’s 8-20; Column 14, lines 19-34, 4041, 54-55, *perturbed, offset*, Column 18, lines 1-5; Column 19, lines 43-67)

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but does not use the term “jitter”. The motivation for combining parallel pipeline processing of graphical images with sampling and filtering with random offset to the coordinates of each pixel rendered in the pipeline is for improved image quality, particularly realism in real-time systems (Deering, Column 2, lines 55-67; Column 3, line 1 through Column 4, line 19).

Dachille discloses the term “jitter” in the context of pipeline processing, and as Examiner understands Applicant Specification (Page 121, left column, second paragraph, line 9). The motivation for combining parallel pipeline processing of graphical images with sampling and filtering, as Dachille discloses (Page 121, lines 3-8), is improve the quality of the image (anti-aliasing). Dachille is evidence that at the time of the invention, it would have been obvious for one skilled in the art of graphics processing to combine the benefits of sampling and filtering, as MacInnis discloses, by “jittering” pixel coordinates, that is by using small random offsets, as Dachille teaches, to improve displayed image quality (anti-aliasing).

### ***Response to Arguments***

20. Applicant’s arguments, see Pages 8-17, filed May 14, 2003, with respect to the rejection(s) of claim(s) 1-14 under 35 U.S.C. Sections 101, 102, 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the judicially created doctrine of provisional obviousness-type double patenting, and Applicant’s amendments necessitated new grounds of rejection.

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***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen E. Quillen whose telephone number is (703) 605-4584.

The examiner can normally be reached on Tuesday – Friday, 8:30am – noon and 1:00 - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella, can be reached on (703) 308-6829.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**Or FAX'd to:**

**(703) 872-9314 (for Technology Center 2600 only)**

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Sixth Floor (Receptionist), Arlington, Virginia

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number (703) 305-9600 or (703) 305-3800.

Allen E. Quillen  
Patent Examiner  
Art Unit 2676

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July 30, 2003



**MATTHEW C. BELLA  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600**